Build notes

4 layers · 1.6 mm nominal finished thickness · 57 × 131.875 mm overall
Green solder mask, white silkscreen, ENIG. Quantity follows the purchase order. Walkie One supplies components; the contracted manufacturer provides fabrication and assembly.

Use the supplied Gerbers and drill files. Manufacture to the Edge_Cuts centerline, including the USB tongue; do not substitute a rectangle. The Gerber stroke bounding box is slightly larger. The outline PDF is a dimensioned reference.

Stack and impedance

Layer / material	Thickness (mm)	Native dielectric data
F.Cu	0.0350	
FR4 3313 RC57% x2 prepreg	0.2064	Dk 4.1 / Df 0.02
In1.Cu	0.0152	
FR4 core	1.0650	Dk 4.6 / Df 0.02
In2.Cu	0.0152	
FR4 3313 RC57% x2 prepreg	0.2064	Dk 4.1 / Df 0.02
B.Cu	0.0350	

Copper plus dielectric: 1.5782 mm; each modeled mask adds 0.010 mm. Native stack reference JLC04161H-3313A identifies the design basis, not a selected manufacturing stack. Actual materials, pressed thicknesses, finished copper and tolerances require process agreement.

Targets: USB 90-ohm differential, main traces 0.2474 mm wide / 0.1524 mm gap; F.Cu references In1.Cu GND, B.Cu references In2.Cu GND. RF 50-ohm single-ended, main traces 0.35 mm on B.Cu over In2.Cu GND. Local escapes differ. Evaluate actual CAM, adjacent copper, launches and transitions with the proposed stack. These are design targets, not measured impedance or USB certification; local USB launch/antipad limitations remain.

Provide predicted impedance and achievable tolerances/coupons with the manufacturing stack. Return any required stack or artwork changes for review; do not silently resize traces, gaps, lands, mask, paste or drills.

Holes and solder mask

415 drilled openings: 412 plated + 3 nonplated. All 396 routing vias have 0.60 mm lands / 0.30 mm drills; twelve U1 thermal holes have 0.60 mm lands / 0.20 mm drills. Four plated USB shell slots complete the plated count. Minimum native track width is 0.15 mm.

Epoxy-fill, planarize and copper-cap all 63 entries in Hole-Maps/fill-cap-common-origin.csv (22 thermal + 41 other exposed vias). Tenting alone is insufficient. Preserve all seven openings in functional-open-common-origin.csv: four USB shell slots, two USB locators and the microphone port. The 0.60 mm microphone NPTH at native (18.25, 49.19) mm must remain free of fill, mask, solder and adhesive.

Twelve ordinary vias beneath modem paste overprint require intact mask tenting; these are separate from the 63 fill/cap entries. U9 has 0.225 mm round copper lands on 0.400 mm pitch, 0.275 mm mask openings and 0.125 mm nominal mask webs. Preserve these individual openings and qualify mask registration.

Assembly notes

137 fitted components: 83 top / 54 bottom; 57 unique MPNs.
Assembly/05E-bom-fitted.csv has 63 grouping rows. Use Assembly/05E-positions-fitted.csv for placements. The board also contains 19 bare test points and nine unpopulated footprints; these are not additional placements.

05E changes: SW1 is now side-actuated B3U-3000P, facing left; it has two solder lands. VOL+ moves 3 mm upward. J10, R6 and R48 are removed; no external temperature-sensor harness is used. RESET/BOOT remain internal top-pressed.

Population, paste and drawings

Do not fit or print paste on: U12, R21, R46, L1, C38, C39, C41, C42, C43. Use only the included WalkieOne-05E-F_Paste.gbr and -B_Paste.gbr as controlled final-deposit artwork. These define final desired deposits, not an approved first-pass stencil recipe; stage-specific tooling must follow the agreed assembly sequence.

Assembly-Drawings.pdf contains both full-board placement maps and ten orientation sheets. Views look directly at each mounting surface. CPL and hole-map X/Y use a common (0,0) origin, X right / Y up; do not add a bottom-side mirror. Native_X/Native_Y in hole maps instead use KiCad Y down. CPL angles are footprint-relative: align machine-library origins and terminals with the actual packages and drawings.

Red reference land 1/A1 does not mean positive. D3 pad 1 is cathode; D1410 pad 1 is common anode; U9 ball A1 is enable. Drawings show lands and holes, not package bodies. Match package markings before placement.

Module reflow limits

U1 (ESP32, top) and U90 (SIM7672G-MNGV, bottom) overlap. Each manufacturer specifies a maximum of one module reflow. An ordinary fully populated two-pass reflow sequence does not meet those limits. A qualified staged/local process with thermal verification for both modules is required. Local heating alone does not establish that the opposite module is protected.

Check supplied module identity, moisture-sensitivity labels, storage and floor life. Apply manufacturer-approved bare-part baking only where required. The package does not prescribe an approved reflow sequence.

Stencil and solder joints

D2 apertures are 0.21 mm rounded squares, radius 0.05 mm. At 0.10 mm foil, D2 area ratio is 0.556 and U9 is 0.625; paste release and solder-paste inspection require qualification. SIMCom guidance specifies 0.15 mm stencil thickness, while retained Hirose U.FL guidance specifies 0.10/0.12 mm. Engineer local thickness/volume compensation and staged tooling; a uniform 0.15 mm bottom stencil is not assumed acceptable.

J1 is GCT USB4105-GF-A. Its 0.95 ±0.15 mm shield stakes do not protrude through the 1.6 mm board. The custom shared ground lands require a qualified solder-addition, inspection and mechanical-retention process for these partial-depth joints.

Handling and process agreement

No board washing or ultrasonic cleaning. Protect the microphone port and nonwashable switches. Provide panel/carrier support and registration/fiducials without interfering with edge controls or the USB tongue; the board has no dedicated panel fiducials/tooling holes. Thermal profile, paste inspection, optical/hidden-joint inspection and the special processes above remain subject to assembler process agreement.

This package supplies fabrication and assembly data. Process or artwork changes must be returned for review before fabrication or assembly.